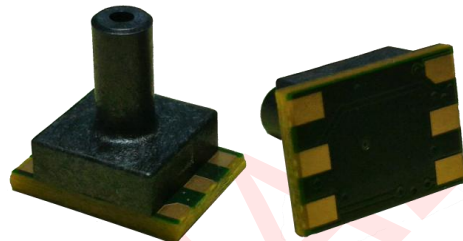**Formosa Measurement Technology Inc. Ltd.**

## *FPS520 series (Preliminary)*
### *Digital pressure sensor*

## Features

- Supply voltage:
  1.7 to 5.5V($V_{DD}$)
  1.2 to 5.5V ($V_{DDIO}$)
- 7, 40, 100kPa pressure range
- 2.2ms fastest conversion time
- Standby current <0.1µA
- $I^2$C and SPI(3-wires) interfaces
- 0-5V analog output
- Calibrated and temperature compensated

## Application Examples

- Water level sensing
- Blood pressure monitor
- Pressure transducer
- Pressure switch
- Medical instrument

## Descriptions

The FPS520 is a new generation of high resolution digital pressure sensor. The FPS520 is a digital pressure sensor which consists of a MEMS piezoresistive pressure sensor and a signal conditioning ASIC. The ASIC include a 24bits sigma-delta ADC, OTP memory for calibration data, and serial interface circuits. The FPS520 could provide both $I^2$C and SPI(3-wires) interface to communicate with microcontroller.

Pressure calibrated and temperature compensated were key features of the FPS520. The data stored in OTP memory could be used to calibrate the FPS520. The calibration procedure should be implemented by a external microprocessor. The FPS520 is low power and supply voltage designed and suitable for portable devices or battery-supplied ones.

## Ordering information

| Part No. | Pressure type | Pressure range | Digital interface | Package | Note |
|---|---|---|---|---|---|
| FPS520-G70HDT | Gauge | 0-7kPa | SPI / $I^2$C | | |
| FPS520-G04KDT | Gauge | 0-40kPa | SPI / $I^2$C | | |
| FPS520-G10KDT | Gauge | 0-100kPa | SPI / $I^2$C | | |

![Formosa Measurement Technology Inc. Ltd. logo]

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## Index of contents

# 1 Functional Block and Pin Descriptions
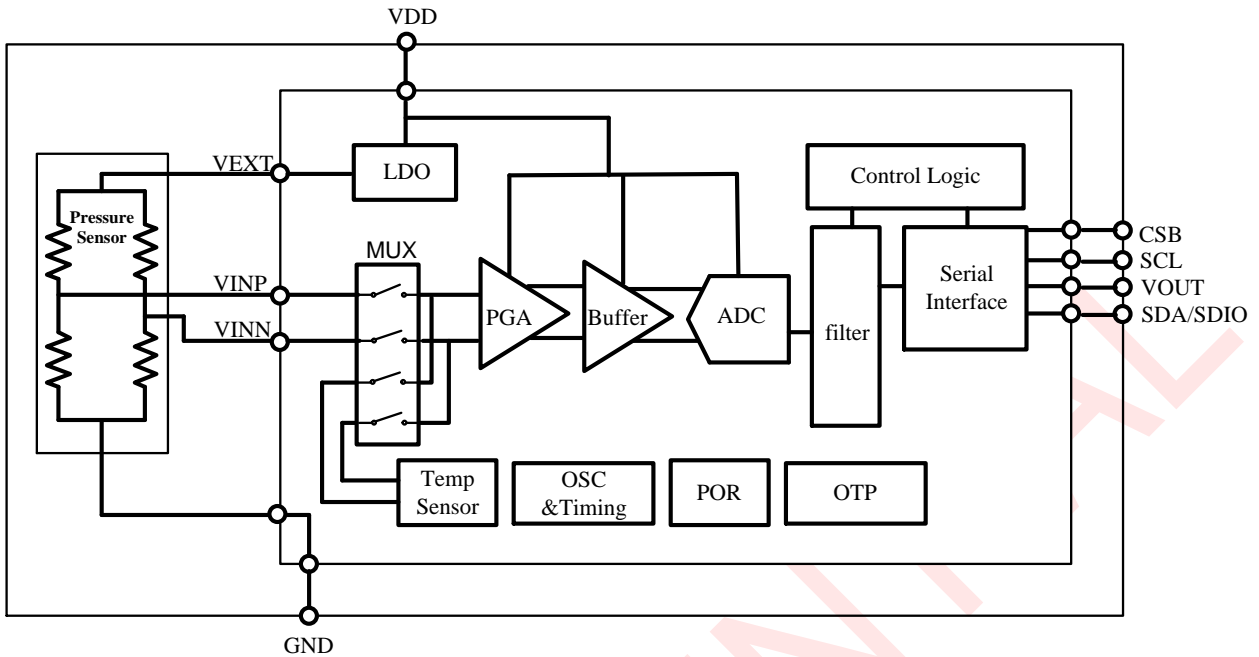


Figure 1.1 Functional Block Diagram of FPS520
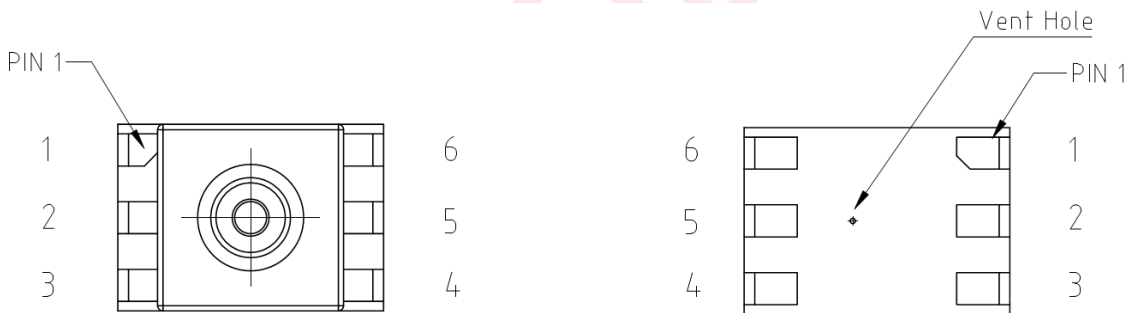


Figure 1.2 Pin definition of FPS520

| Pin No. | Pin Name | Description |
|---------|----------|-------------|
| 1 | SCL | Serial clock |
| 2 | SDA/SDIO | Serial data input/output in $I^2C$ mode(SDA) <br> Serial data input/output in 3-wire SPI mode (SDIO) |
| 3 | CSB | Chip Select |
| 4 | $V_{DD}$ | Power supply for core circuits |
| 5 | VOUT | Analog output |
| 6 | GND | Ground |

# Formosa Measurement Technology Inc. Ltd.

## 2 Electrical Characteristic

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Pressure Range<br>FPS520-G70HDT<br>FPS520-G04KDT<br>FPS520-G10KDT | | | <br>0<br>0<br>0 | | <br>7<br>40<br>100 | kPa | |
| Operating Temperature Range | | | -40 | | 85 | °C | |
| Supply Voltage | $V_{DD}$ | | 1.7 | 1.8 | 5.5 | V | |
| | $V_{DDIO}$ | | 1.2 | 1.8 | 5.5 | V | |
| Supply Current<br>Pressure measurement<br> Ultra low power<br> Standard<br> High resolution<br> Ultra high resolution<br> Temperature measurement | $I_{DD}$ | $V_{DD}$=2.5V<br>1 conversion/sec. | | <br><br>3.0<br>4.7<br>7.7<br>13.9<br>1.9 | <br><br>3.5<br>6.4<br>8.9<br>16.0<br>2.2 | µA | |
| Peak Current During Conversion<br>Pressure measurement<br>Temperature measurement | $I_{peak}$ | $V_{DD}$=2.5V | | <br>1.51<br>0.95 | | mA | |
| Standby Current | $I_{sd}$ | | | <0.1 | | µA | |
| Conversion time<br>Pressure measurement<br> Ultra low power<br> Standard<br> High resolution<br> Ultra high resolution<br> Temperature measurement | | | | <br><br>2.2<br>3.3<br>5.4<br>9.8<br>2.2 | <br><br>2.5<br>3.7<br>6.0<br>10.7<br>2.5 | ms | |
| Relative Pressure Accuracy<br>$V_{DD}$=3.3V | | 65~85℃<br>0~65℃<br>-20~0℃<br>-40~-20℃ | -1 | ±0.5 | 1 | %FS | 2 |
| Absolute Pressure Accuracy<br>$V_{DD}$=3.3V | | 65~85℃<br>0~65℃<br>-20~0℃<br>-40~-20℃ | -2<br>-1.5<br>-2.5<br>-3.5 | ±1<br>±0.5<br>±1.5<br>±2 | 2<br>1.5<br>2.5<br>3.5 | %FS | 3 |
| Noise in pressure (7kPa)<br> Ultra low power<br> Standard<br> High resolution<br> Ultra high resolution | | | | 0.664<br>0.482<br>0.361<br>0.268 | | Pa | RMS noise |
| Noise in pressure (40kPa)<br> Ultra low power<br> Standard<br> High resolution<br> Ultra high resolution | | | | TBD | | Pa | RMS noise |
| Noise in pressure (100kPa)<br> Ultra low power<br> Standard<br> High resolution<br> Ultra high resolution | | | | TBD | | Pa | RMS noise |
| Absolute temperature accuracy<br>$V_{DD}$=3.3V | | @25℃<br>0~65℃ | -1.5<br>-2 | ±0.5<br>±1 | 1.5<br>2 | ℃ | |
| Soldering drift | | After solder reflow | | TBD | | | |
| Long term stability | | 12 months | | TBD | | | |

1. All the data were measured with 2.5V supply voltage at a temperature of 25±3℃, unless otherwise noted.
2. Maximum error of pressure reading over the pressure range after offset adjusted at one pressure point.

3. Maximum error of pressure reading over the pressure range.

4. According to 32 bit integer compensation formula.

# 3 Absolute Maximum Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | AVDD | | -0.3 | | 6.5 | V | |
| | VDDIO | | -0.3 | | 6.5 | V | |
| Digital output voltage | | | -0.3 | | VDDIO+ 0.3 | V | |
| Storage Temperature Range | | | -40 | | 125 | $^{o}$C | |
| Maximum Overpressure | | | | | 10 | bar | |
| ESD Rating HBM | | | | 2 | | kV | |

# 4 Application Information

Owing to state of the art, the FPS520 build a new standard of digital barometer. A 24bits sigma-delta ADC and a MEMS pressure sensor are integrated in a LGA substrate. Pressure calibrated and temperature compensated were key features of the FPS520. The FPS520 is low power and supply voltage designed and suitable for portable devices or battery-supplied ones.

The data stored in OTP memory could be used to calibrate the FPS520. The calibration procedure should be implemented by a external microprocessor. By I$^2$C or SPI interface, you can get the calibration data stored in OTP and the raw data of pressure and temperature. In order to get the correct pressure and temperature reading, the calculating procedure must be implemented in a microprocessor.
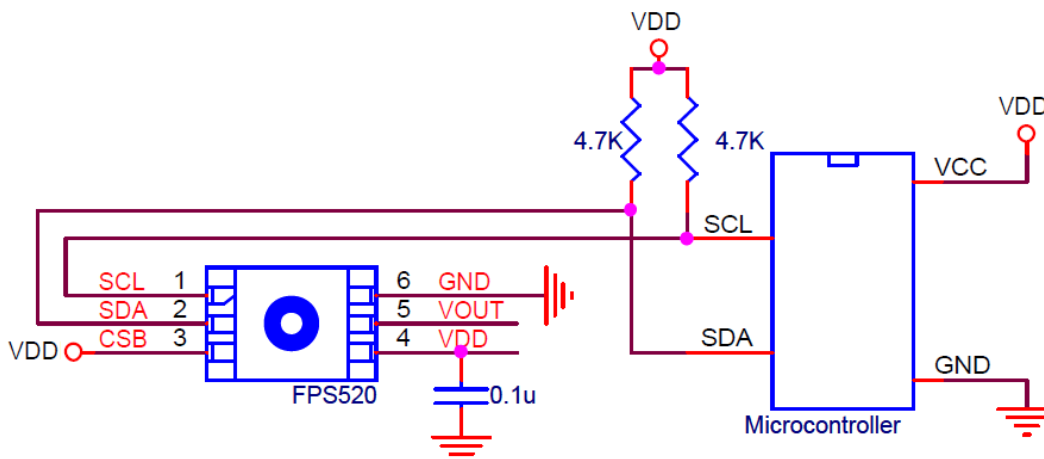
**Application Circuit example**



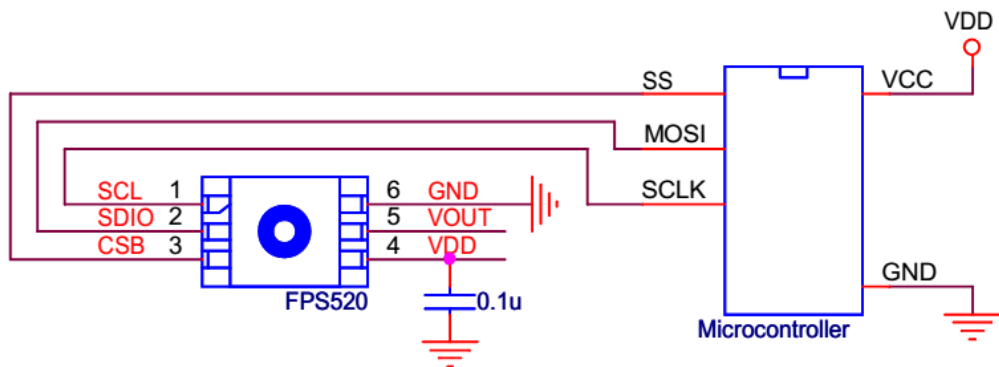Figure. 4.1 Application circuit for I$^2$C interface

Figure 4.2 Application circuit for SPI interface

# 5 Control registers

Table 5.1 control registers

| Addr | Description | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|-------------|-----|------|------|------|------|------|------|------|------|---------|
| 0xF8 | DATA_LSB | R | Data out<7:0> | | | | | | | | 0x00 |
| 0xF7 | DATA_CSB | R | Data out<15:8> | | | | | | | | 0x00 |
| 0xF6 | DATA_MSB | R | Data out<23:16> | | | | | | | | 0x00 |
| 0xF4 | CONFIG_1 | RW | OSR<1:0> | | Measurement_control<5:0> | | | | | | 0x00 |
| 0xF1 | Cal_coeff | R | Calibration Registers | | | | | | | | N/A |
| 0xE0 | Soft_reset | W | Softreset<7:0> | | | | | | | | 0x00 |
| 0xD0 | Cal_coeff | R | Calibration Registers | | | | | | | | N/A |
| 0xBB-0xAA | Cal_coeff | R | Calibration Registers | | | | | | | | N/A |
| 0x6B | Part ID | R | PartID<7:0> | | | | | | | | 0x42 |
| 0x00 | SPI_Ctrl | RW | SDO_active | LSB_first | | | | | LSB_first | SDO_active | 0x00 |

**Reg 0xF6–0xF8**

    **Data_out:** 24 bits ADC output data

**Reg 0xF4**

    **OSR<1:0>:** 00:1024X, 01:2048X, 10:4096X, 11:8192X

    **Measurement_control<5:0>:** 101110, indicate a temperature conversion. 110100, indicate a pressure conversion.

**Reg 0xE0**

    **Softreset** : Write only register. If set to 0xB6, will perform a power on reset sequence. Auto returned to 0 after the soft reset completed.

**Reg {0xF1, 0xD0, 0xBB:0xAA}**

**Calibration Registers** : Total 20bytes calibration registers used for sensor calibration.

**Reg 0x6B**

**PartID:** 8 bits Part ID, the default value is 0x42.

**Reg 0x00**

**SDO_active:** 1: 4-wire SPI, 0: 3-wire SPI (FPS520 only support 3-wires operation)

**LSB_first:** 1: LSB first for SPI interface, 0: MSB first for SPI interface

Table 5.2 Summary of instructions

| Instruction | Register address | Value |
|---|---|---|
| Pressure measurement, OSR1024 | 0xF4 | 0x34 |
| Pressure measurement, OSR2048 | 0xF4 | 0x74 |
| Pressure measurement, OSR4096 | 0xF4 | 0xB4 |
| Pressure measurement, OSR8192 | 0xF4 | 0xF4 |
| Temperature measurement | 0xF4 | 0x2E |
| Softreset | 0xE0 | 0xB6 |
| 3-wire SPI, MSB first | 0x00 | 0x00 |
| 4-wire SPI, MSB first | 0x00 | 0x81 |

# 6  SPI Interface

FPS520 provides both SPI(3-wires) and I$^2$C interface for serial communication and 'CSB' pin is used to switch between these two protocols. Pulling 'CSB' pin low selects the SPI interface, leaving 'CSB' pin float or pulling it high selects the I$^2$C interface. The SPI interface is compatible with SPI mode 0 (CPOL=0, CPHA=0). FPS520 support only 3-wires SPI operation.

Table 6.1 SPI interface specifications

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{sclk}$ | Clock frequency | Max load on SDIO or SDO = 25pF | | 10 | MHz |
| $t_{sclk\_l}$ | SCLK low pulse | | 20 | | ns |
| $t_{sclk\_h}$ | SCLK high pulse | | 20 | | ns |
| $T_{sdi\_setup}$ | SDI setup time | | 20 | | ns |
| $T_{sdi\_hold}$ | SDI hold time | | 20 | | ns |
| $T_{sdo\_od}$ | SDO/SDI output delay | Load = 25pF | | 30 | ns |
| | | Load = 250pF | | 40 | ns |
| $T_{csb\_setup}$ | CSB setup time | | 20 | | ns |
| $T_{csb\_hold}$ | CSB hold time | | 40 | | ns |

The figure below shows the definition of the SPI timing given in table 6.1
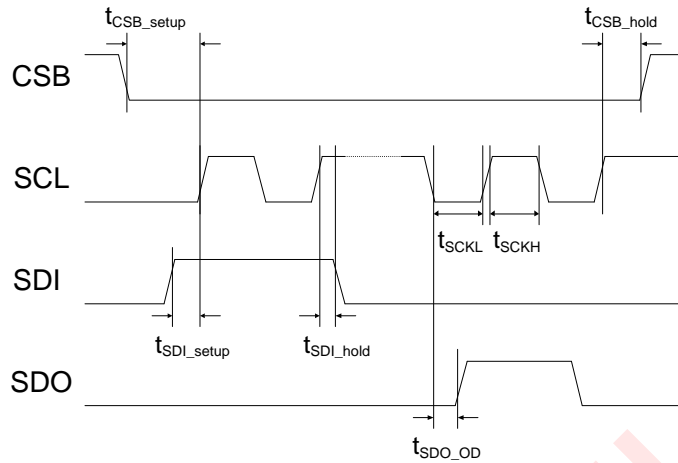


Figure 6.1 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 6.2, the instruction phase is divided into a number of bit fields.
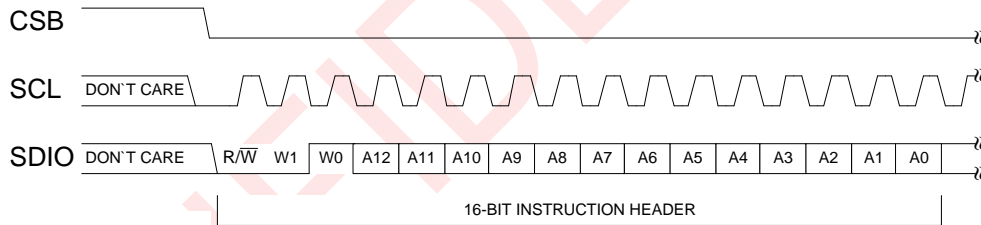


Figure 6.2 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 6.2). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a nonbyte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 6.2 W1 and W0 settings

| W1:W0 | Action | CSB stalling |
|-------|--------|--------------|
| 00 | 1 byte of data can be transferred. | Optional |
| 01 | 2 bytes of data can be transferred. | Optional |
| 10 | 3 bytes of data can be transferred. | Optional |
| 11 | 4 or more bytes of data can be transferred. CSB must | No |

| be held low for entire sequence; otherwise, the cycle is terminated. | |
|---|---|

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. (Figure 6.3)
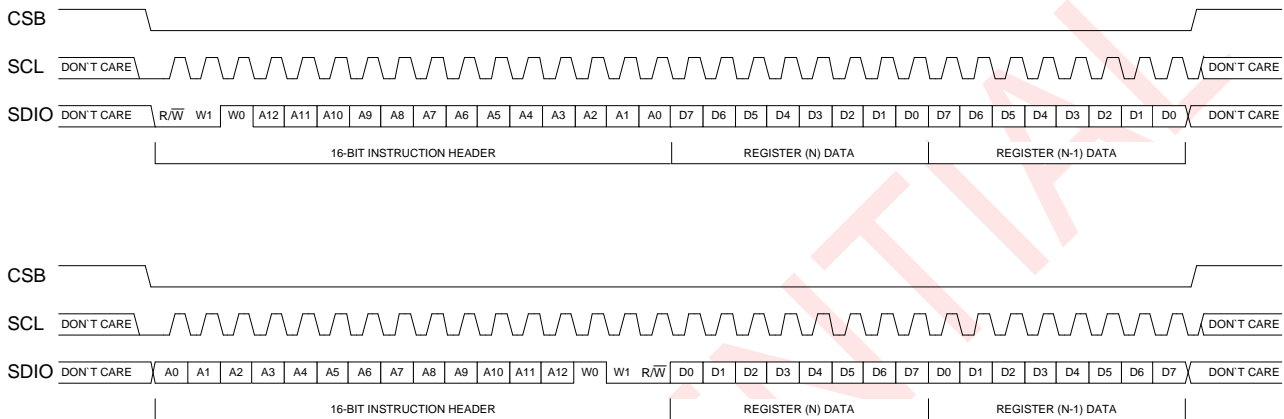


Figure 6.3 MSB First and LSB First Instruction and Data Phases

# 7   I$^2$C Interface

I$^2$C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I$^2$C device address of FPS520 is shown below. And the device address is "1101100". For I$^2$C bus application,' CSB' pin have to be left float or pulled high.

Table 7.1 I$^2$C Address.

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | W/R |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0/1 |

Table 7.2 Electrical specification of the I$^2$C interface pins

| Symbol | Parameter | Condition | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
| $f_{scl}$ | Clock frequency | | | 400 | kHz |
| $t_{LOW}$ | SCL low pulse | | 1.3 | | us |
| $t_{HIGH}$ | SCL high pulse | | 0.6 | | us |
| $t_{SUDAT}$ | SDA setup time | | 0.1 | | us |
| $t_{HDDAT}$ | SDA hold time | | 0.0 | | us |

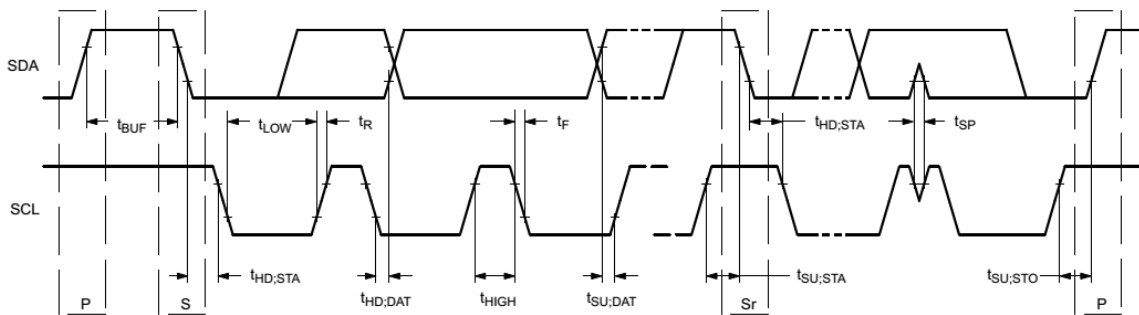| $t_{SUSTA}$ | Setup Time for a repeated start condition | | 0.6 | | us |
|---|---|---|---|---|---|
| $t_{HDSTA}$ | Hold time for a start condition | | 0.6 | | us |
| $t_{SUSTO}$ | Setup Time for a stop condition | | 0.6 | | us |
| $t_{BUF}$ | Time before a new transmission can start | | 1.3 | | us |



Figure 7.1 $I^2$C Timing Diagram

The $I^2$C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.
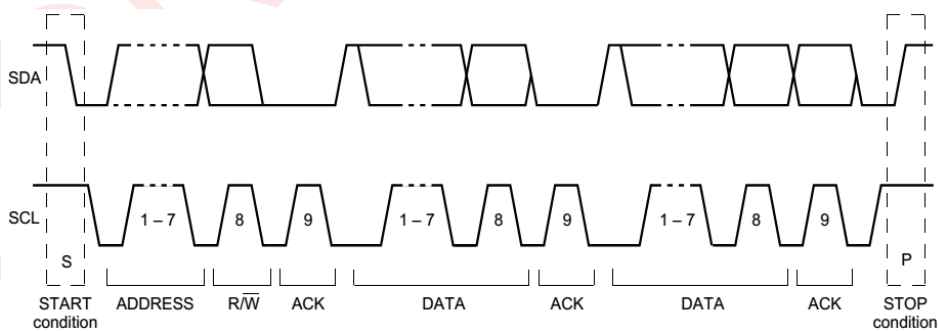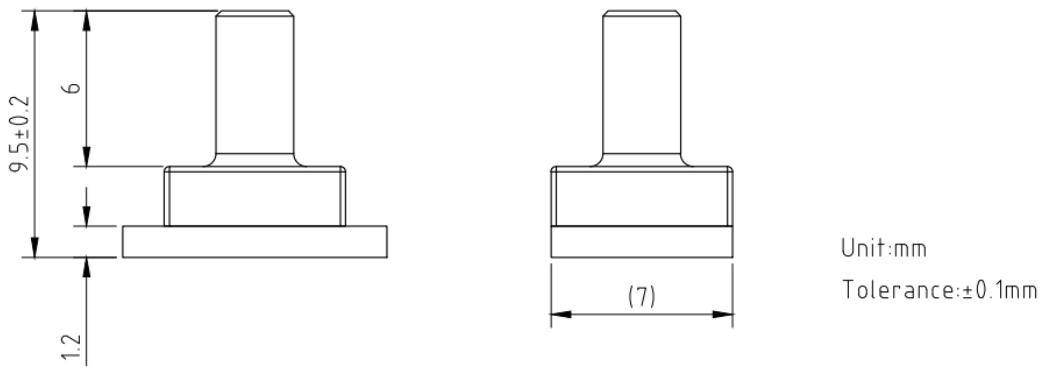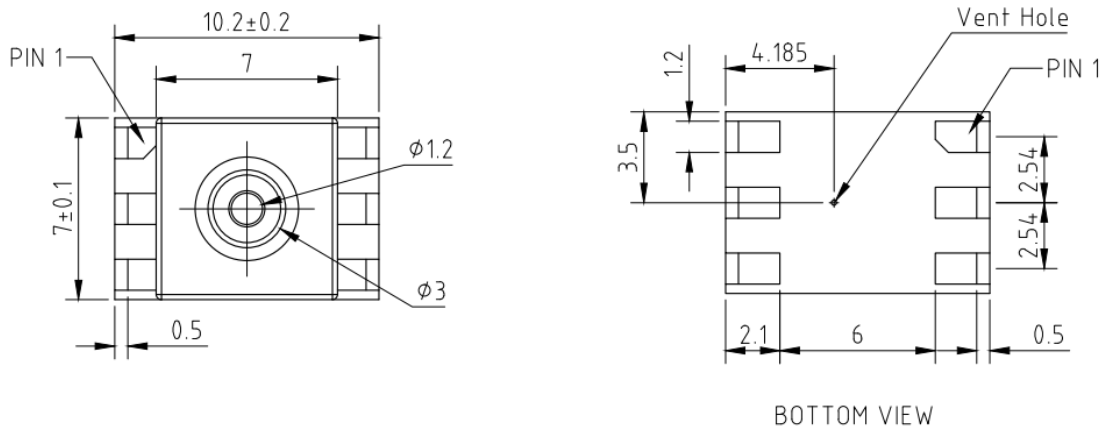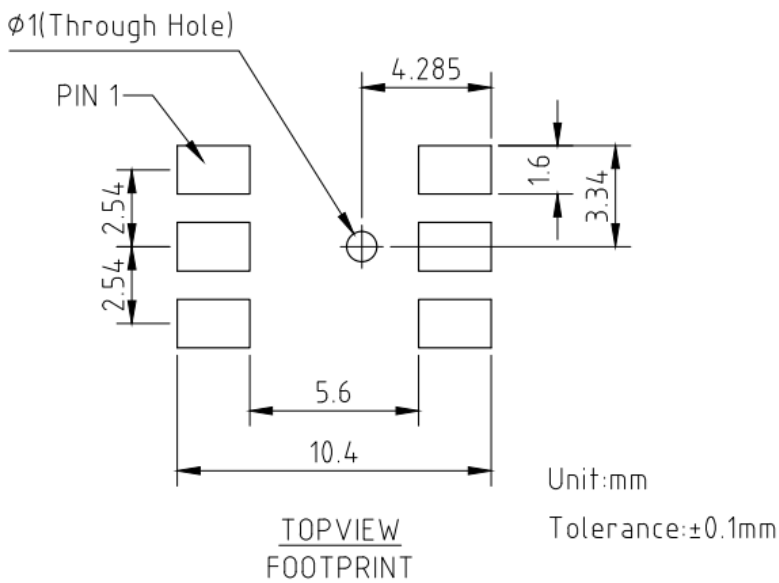


Figure 7.2 $I^2$C Protocol

# 8   Package Information

## 8.1   Outline dimensions



BOTTOM VIEW

Unit:mm
Tolerance:±0.1mm

## 8.2   Recommended footprint



TOPVIEW
FOOTPRINT

Unit:mm
Tolerance:±0.1mm

**Formosa Measurement Technology Inc. Ltd.**

# 9 Document history and modification

| Rev. | Description | Date |
|------|-------------|------|
| 0.1 | First edition (preliminary) | 2015/10/16 |
| 0.2 | Modified: | 2016/6/7 |
| |     Product picture, page 1 | |
| |     Figure 1.2 Pin definition of FPS520, page 3 | |
| |     Application circuit example, page 5, 6 | |
| |     SDO_active, page 7 | |
| |     I2C address, page9 | |
| |     8.1 Outline dimensions, page 11 | |
| |     8.2 Recommended footprint, page 11 | |
| | Deleted: | |
| |     Figure 6.4, page 9 | |
| 0.3 | Modified: | 2016/6/23 |
| |     8.1 Outline dimensions, page 11→Tolerance | |
| 0.4 | Modified: | 2016/12/15 |
| |     Product picture, page 1 | |
| |     8.1 Outline dimensions, page 11 | |
| |     8.2 Recommended footprint, page 11 | |